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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,210	12/31/2003	Edward Brian Boles	068354.1411	3407

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PATENT DEPARTMENT
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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,210	BOLES ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 2 and 7 rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 2 of prior U.S. Patent No. 6,708,268. This is a double patenting rejection.

Patent 6,708,268	Instant application
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank,	2. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank,

Patent 6,708,268 (claim 1 continued)	Instant application (claim 2 continued)
whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file;	whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file;
an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory,	an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory,
wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory;	wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory;
and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;	and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;
wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.

Patent 6,708,268 (claim 2)	Instant application (claim 7)
2.A microcontroller comprising: a central processing unit; a data memory coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory, wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit.	7.A microcontroller comprising: a central processing unit; a data memory coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory, wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 3-6 and 8-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The subject matter of claims 3-6 and 8-11 are directed to an encoding of data which is merely particular sets of bits. The

data is detailed as instructions and certain bits are used to modify the behavior of the instruction (claim 3) or provides (claim 4) an unconditional branch for a program for a program composed from said instruction set any where with in 2 megabyte range designated by said kkkk and kkkk kkkk kkkk portions of said instruction. The particular provision of an encoding of bits does not provide any tangible result and the claims merely state an intended use for the encoded data. Likewise the encoding of instruction data claimed as instructions in claims 5,6,8,9,10,11 set forth an encoding of bits that do not set forth or produce any tangible result. These claims are directed toward abstract ideas. The independent claims although part of the dependent claims and set forth an apparatus, are not the inventive concept in the dependent claims. The particular encoding of data is the inventive concept in the dependent claim. The particular encoding of a set bits is an abstract idea and not statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8-11 recite the limitation "said instruction set" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER